Monolithically integrated 112 Gbps PAM4 optical transmitter and receiver in a 45nm CMOS-silicon photonics process

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Abstract: We demonstrate a transmitter and receiver in a silicon photonics platform for O-band optical communication that monolithically incorporates a modulator driver, traveling-wave Mach-Zehnder modulator, control circuitry, photodetector, and TIA in the GlobalFoundries Fotonix™ (45SPCLO) platform. The transmitter and receiver show an open 112 Gbps PAM4 eye at a 4.3 pJ/bit energy efficiency, not including the laser. Extensive use of gain-peaking enables our modulator driver and TIA to achieve the high bandwidths needed in the 45 nm CMOS-silicon photonics process. Our results suggest an alternative to the frequent approach of bump-bonding BiCMOS drivers and TIAs to silicon photonics.

1. Introduction

Performance per Watt is one of the critical metrics by which a computer system is judged. The numerator, performance, is typically expressed as the number of operations per second performed when the computer system is operating at peak throughput. The denominator, Watts, is the overall power consumption of the system during this period. Power dissipated in the processors, switches, communication links, power supplies, memory, cooling systems, and associated supporting infrastructure all contribute to the denominator. As overall bandwidths increase, the power required for data movement in an exascale computing system becomes a significant contributor to the power consumption of a system. Existing systems implement more than 1000 Pbps of total memory bandwidth [1]. A future disaggregated memory system could see further scaling with a significant fraction of the bandwidth transmitted in the optical domain [2]. In terms of energy efficiency of such links, an end-to-end optical link using pluggable optics may consume on the order of 25 pJ/bit, including the SERDES in the host ASIC [3]. At 2000 Pbps of bidirectional traffic and 25 pJ/bit, the power dissipated in optical links would multiply to 50 MW for such an optically-connected memory system, significantly more than the entire system power of existing Top500 HPC systems [4]. Here, we have ignored the power from optical links to support switching and other functionality to express orders-of-magnitude. It follows that continued bandwidth scaling for new computer architectures will require further improvements in the energy efficiency of optical links in order to preserve or improve performance per Watt.
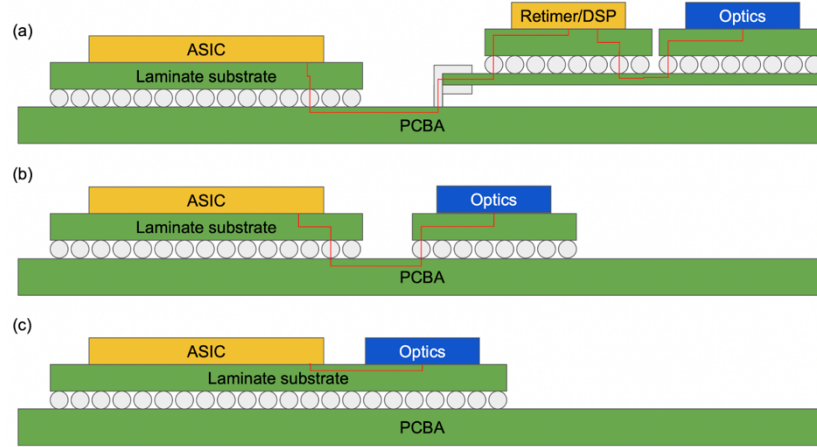
Fig. 1. (a) A conventional optical link from an ASIC on a host PCB to a pluggable optical module with a retimer or DSP chip. (b) An alternative link in which the optical engine is placed in a package near the ASIC, (c) Co-packaged optics in which the optical engine is on the same substrate as the ASIC. The arrangements shown in (b) and (c) provide net power consumption savings over (a) by eliminating the retimer/DSP chip.

Co-packaged optics improves the performance per Watt of computer systems by eliminating the need for additional electrical retimer chips, such as those used in conventional pluggable optics. Fig. 1(a) shows an illustration of the electrical connectivity from a host ASIC (a switch or processor, for example) to a pluggable optical module that provides the interface to optical fibers. Inside of the pluggable module, it is common to include a DSP chip, which converts the host-side interface, such as 8x50 Gbps signaling, into an optical interface, such as 4x100 Gbps signaling [5]. Crucially, the DSP chip also provides retiming and equalization functionality, as closing the full link from the ASIC through the pluggable connector to the optics directly would be too challenging. Fig. 1(b,c) shows example links in which the DSP chip is not required. In (b), the separately-packaged optical engine is located near the ASIC, similar to the orientation inside of the pluggable, while in (c), the optical engine and the ASIC are co-packaged together. While both (b) and (c) eliminate the DSP chip, the co-packaged solution requires less signal equalization, which in turn can lead to improved optical sensitivity and/or lower electrical power consumption within the SERDES.

The requirements of a co-packaged optical link motivate a technology that can support high-density I/O and excellent energy efficiency [6,7]. To meet these needs, silicon photonics (SiPh) emerges as a promising platform for next-generation interconnects because of the ease with which it is possible to take advantage of existing multi-chip module assembly infrastructure [8,9]. In particular, a monolithic CMOS+SiPh process is ideal for CPO because it enables: (1) Device density that exceeds conventional pad-pitch limitations of wirebond, flip-chip, or advanced packaging techniques, (2) simplified electrical assembly compared to heterogeneous electrical amplifier and photonics chipsets, and (3) close integration between ASICs and optical I/O [10-12].

However, one large disadvantage of a monolithic CMOS-SiPh process is that, typically, the performance of the CMOS is not state-of-the-art [13]. Thus, an open question exists whether such monolithic CMOS-SiPh processes can enable optical links at the latest-generation of bit rates, modulation formats, and SERDES capabilities. Importantly, for most chip-to-chip communications inside of exascale compute systems, this typically requires interoperability with the interfaces that support PCB or backplane communications. If a link can be connected electrically rather than optically, it typically should from an energy & cost perspective. It is also desirable to be able to use a single ASIC design for both electrical

connectivity and optical connectivity. Thus, interfacing optics to ASICs at the latest generation of standard 112 Gbps, or similar, rates enables a flexible I/O architecture.

Designing both a transmitter and a receiver in a monolithic CMOS-SiPh process at these data rates is as of yet undemonstrated in literature. Many results have demonstrated heterogeneous chipsets integrated in a 2D, 2.5D, or 3D assembly with separate electrical ICs and photonic ICs [3, 5, 14-21]. Prior monolithic literature with both a transmitter and receiver on-wafer demonstrated links at up to 25 Gbps [22-24] with published simulation models for a monolithic die at 106 Gbps [25]. Prior individual monolithic results (i.e., only a transmitter or only a receiver) demonstrate a transmitter at 44 Gbps NRZ [26], a receiver at 56Gbps NRZ [27], and a coherent receiver at up to 66 Gbaud QPSK [28], all in a SiGe BiCMOS-SiPh monolithic process; as well as a 100 Gbps PAM4 transmitter [29], a 56 Gbps PAM4 transmitter [30], and separately a 28 Gbps NRZ receiver [31] in a CMOS-SiPh process.

In this manuscript, we describe in detail the first CMOS-SiPh monolithic transmitter and receiver for 112 Gbps optical communication designed and fabricated in the GlobalFoundries Fotonix™ (45SPCLO) platform. The chips operate near 1310 nm and monolithically incorporate all the electrical and optical functionality for an optical transmitter and receiver, except for the laser which is packaged separately and fiber-coupled. The transmitter (TX) and receiver (RX) photonic-analog chips (PAC) are fabricated on the same wafer without any process modifications between the two designs. The TX PAC comprises a linear modulator driver, traveling-wave Mach-Zehnder (TWMZ) modulator, an integrated feedback control system, and digital serial peripheral interface (SPI). The RX PAC comprises an integrated photodetector, linear transimpedance amplifier (TIA), and a separate SPI bus. Both the TX PAC and RX PAC are shown to operate with open eyes at 112 Gbps PAM4.
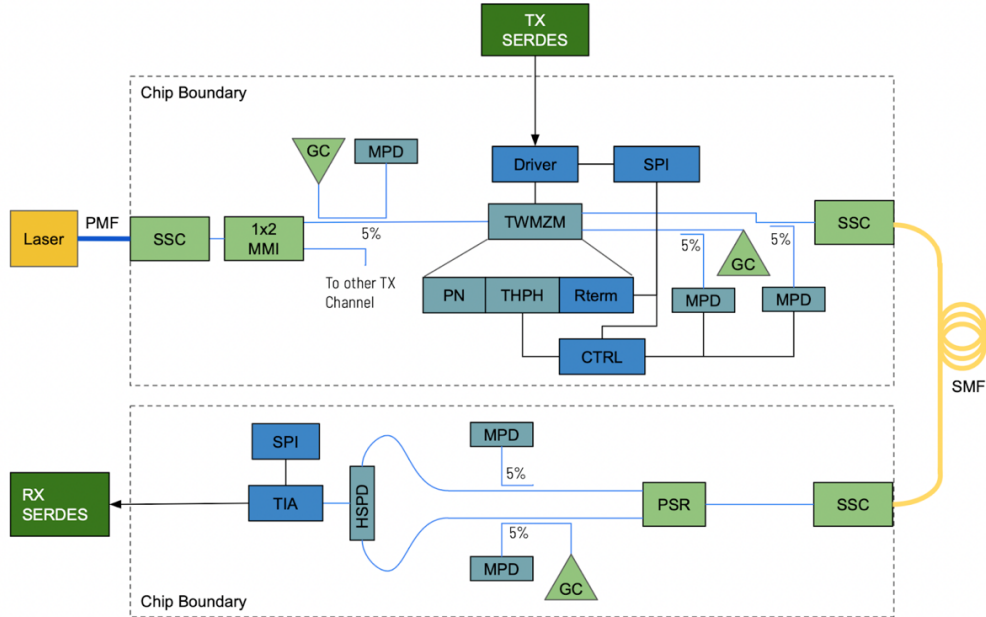

Fig. 2. Schematic representation of the on-chip signal path, including spot-size converter (SSC), 1x2 laser splitter, monitor photodiodes (MPD), serial peripheral interface (SPI) for control, traveling wave Mach-Zehnder modulator (TWMZM), high-speed pn-junction phase shifter (PN), thermal phase shifter (THPH), adjustable termination resistor (Rterm), high-speed photodetectors (HSPD), polarization splitter & rotators (PSR), grating couplers for testing (GC), and integrated control system (CTRL).

2. Design and Fabrication

The transmitter and receiver are designed as separate chips on the same reticle and wafer. No process splits are utilized between the two chips. Each TX PAC contains 16 channels with 8 total laser inputs where each laser is split two ways. Each RX PAC also contains 16 channels with on-chip polarization diversity. V-groove edge couplers are used as spot-size converters between optical fibers and on-chip waveguides [12]. Grating-couplers are used throughout both chips for wafer-level and some chip-level testing. Refer to Fig. 2 for a schematic representation of the on-chip signal paths.

A current mode driver chain is used to drive a differential TWMZ that is terminated by an adjustable termination resistor [32]. The pn junctions in each arm are each driven in push-pull configuration and see the full drive voltage, with an overall differential transmission line [33,34]. Therefore, the driver is designed to be loaded by a 24 Ω differential impedance transmission line and provide 1.6 V peak-to-peak differential voltage. In combination with the modulator, the TX PAC is calculated to achieve a low-frequency phase shift of 1.1 radians. During operation, applied equalization will lower the total modulation depth. The driver chain consists of an input termination followed by 5 CML stages. The input of the driver chain is matched to a 100 Ω differential resistor and DC coupled with a common mode voltage of 650 mV.

All driver stages are CML-based amplifiers with different functionalities, as shown in Fig. 3(a). The input stage is sized to provide minimum capacitive loading at the input to achieve low input return loss. The second stage is a CTLE with switchable RC source degeneration to provide high frequency peaking for bandwidth improvement. The third stage is a variable gain amplifier (VGA) to adjust the driver gain. The input termination and CML stages benefit from T-coils at their output to improve the bandwidth. The last stage of the driver, shown in Fig. 3(b), is a cascode CML stage with thick oxide FETs as output devices to tolerate high output swing. In order to achieve the optimal linear swing, the output stage is powered using a 1.8 V supply. The driver is double-terminated with adjustable resistors to reduce the reflections at both ends. However, the termination on the driver side must be kept higher to preserve the voltage swing amplitude. Fig. 3(c) plots the simulated |EOS21| response of the PAC-TX from driver input to fiber output at nominal process and temperature corners.

The RX lane architecture is shown in Fig. 4(a). An illuminated single-ended photodiode drives a balanced RX implementation. A dark photodiode is connected to the complementary RX input. The first stage is a pseudo-differential inverter-based shunt-feedback TIA, followed by an inverter-based Cherry-Hooper amplifier. Both inverter-based stages have symmetric T-coil inductive peaking [35] and are powered by an externally regulated low-noise power supply. The subsequent stages are implemented as fully differential CML-based amplifiers with no supply regulation. The first CML stage performs single-ended to differential (S2D) conversion, followed by a programmable continuous-time linear equalization (CTLE), a programmable gain amplifier (PGA), a pre-driver, and an output pad driver. Most CML stages use bridged-shunt inductive peaking networks, chosen for robustness, while the pad driver has a symmetric T-coil network for broadband output matching [36].
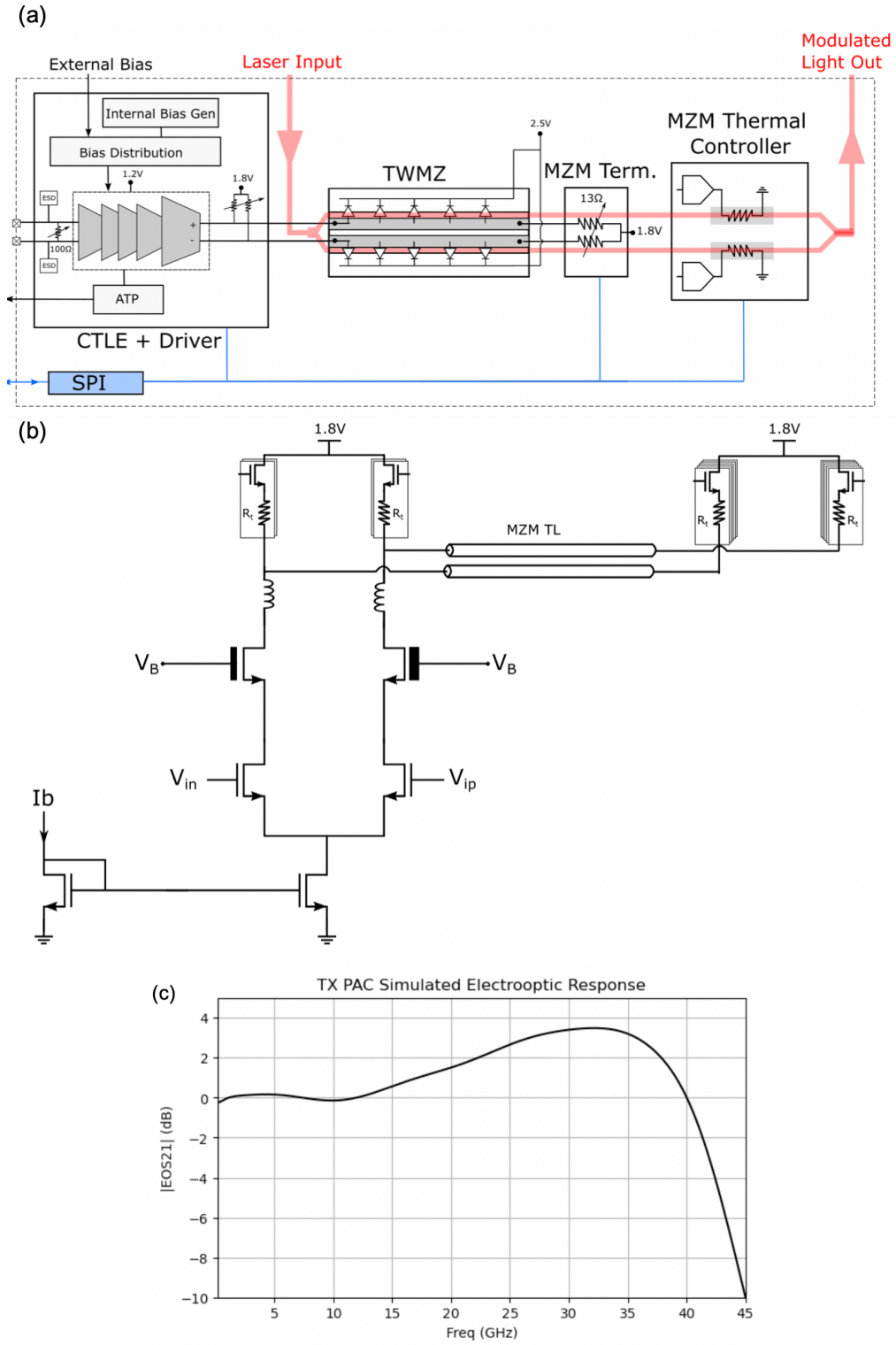
Fig. 3. (a) Modulator driver architecture, (b) output driver stage schematic diagram, and (c) simulated |EOS21| response of the TX PAC.

Independent common-mode feedback circuits sense the output of each Cherry-Hooper amplifier and feed back a DC current into the respective photo-detector anode. This scheme allows for optimal S2D input common-mode biasing, and the use of independent voltage references allow for foreground offset calibration. The low-pass filter cut-off is lower than 50 kHz, resulting in negligible baseline wander at 112 Gbps. On-chip current and voltage generators bias the RX, and an SPI interface allows for digital programming of internal registers. At high gain, simulated noise at 30 GHz is 17.7 pA/Hz$^{1/2}$. Fig 4(b) plots the simulated AC response at three different gain settings.
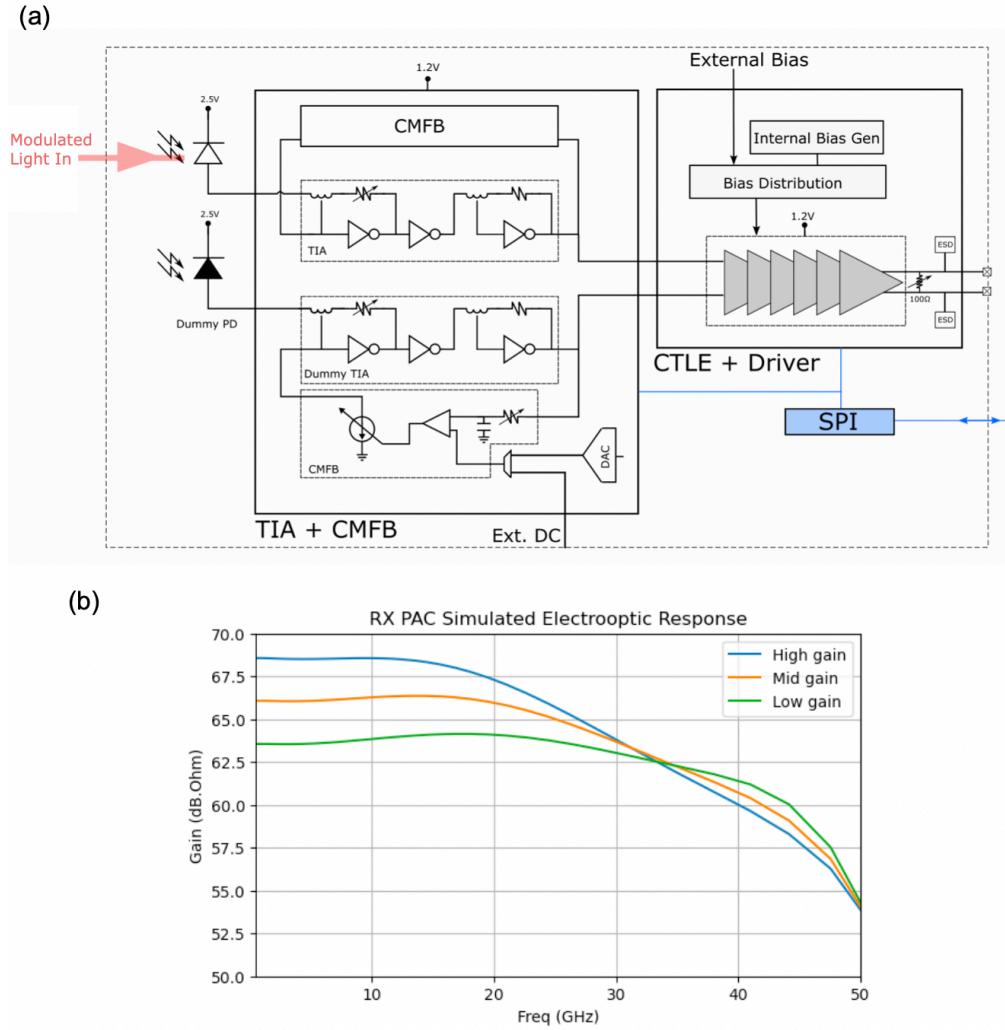
(a)

(b)

Fig. 4. (a) TIA & pad driver architecture and (b) simulated AC response of the PAC RX TIA loaded with the photodetector at three different gain settings.

The wafers are fabricated in GlobalFoundries' 300 mm 45 nm SOI process (GF Fotonix™). The wafers monolithically integrate high-speed transistors, modulators, photodetectors, ridge waveguides, rib waveguides, silicon nitride waveguides, V-groove edge couplers, and a full metal stack.

3. Experimental Results

The transmitter and receiver chips are designed for co-packaged applications wherein the full-flow wafers are bumped with V-groove edge couplers and the high-speed I/O are directly connected to the host ASIC SERDES. High-speed probes are used for testing the individual performance of the transmitter and receiver since the flip-chip substrate application circuit limits access to the high-speed inputs and outputs of the chip. Fig. 5. shows photographs of the full transmitter and receiver chips, as well as the devices under test. The TX PAC uses a separate glass array of polarization-maintaining fibers for laser inputs and standard single-mode fibers for modulator outputs. The RX PAC uses a single array of standard single-mode fiber. The low-speed I/O and power supplies are connected via wirebonds to a printed circuit board while the high-speed I/O is probed in a ground-signal-signal-ground configuration for both TX and RX PACs.
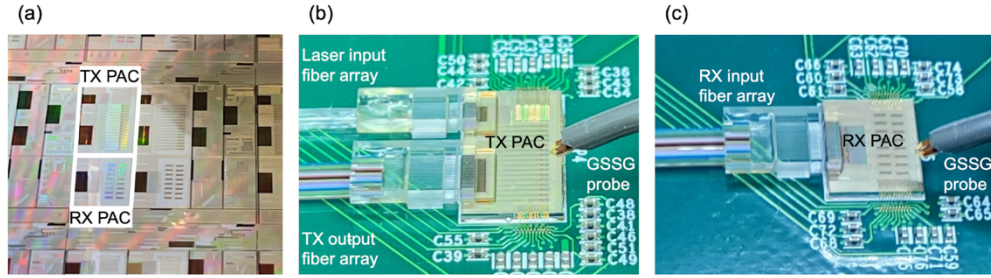

Fig. 5. Photographs of (a) the TX and RX chips on-wafer, (b) the TX PAC under test, and (c) the RX PAC under test.

Fig. 6 shows a block diagram of the transmitter and receiver test setups. A Keysight M8194A arbitrary waveform generator (AWG) generates the high-speed PAM4 signal, while a Keysight DCA-N1092C oscilloscope (DCA) captures the signal. An FPGA and microcontroller are used to communicate to the on-chip SPI and external DC power supplies provide power and biasing. For receiver characterization, an external EOSpace 40 GHz lithium niobate modulator is used to generate the input optical waveform. For all testing, the laser outputs near 1310nm.

The TX PAC is tested with a 50mW input in the PM fiber. On-chip, each laser input is split once so that each channel requires approximately 25mW of laser power. The PDFA optical amplifier is used to amplify the Tx output to approximately 0 dBm before entering the DCA. During operation, the on-chip control loops bias and stabilize the thermal tuner inside the TWMZ. A SPI command is used to flip a single polarity bit that determines whether the control loop stabilizes on a rising edge or falling edge of the Mach-Zehnder transfer function. On-chip ADCs, DACs, low-speed TIAs, and low dropout voltage regulators sample the MPD photocurrent and drive the thermal tuners. During transmitter output eye diagram characterization, the s-parameter response for the 1.85 mm cabling up to the probe input (but not including the probe or TX PAC) is equalized from the AWG output. A 5-tap T-spaced feed forward equalizer is then optimized & applied at the AWG to compensate for the probe and TX PAC electro-optic response. The measured fiber-to-fiber insertion loss of the transmitter when biased at the maximum TWMZ transmission point is 15.3 dB; we note this includes an intrinsic 3 dB loss for splitting each laser into two channels.
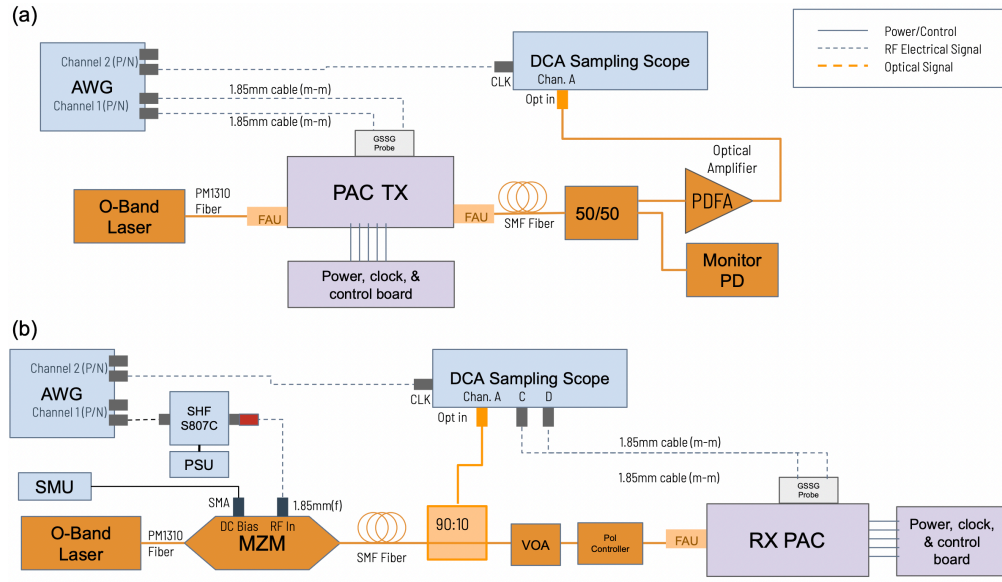
Fig. 6. Block diagram of the (a) transmitter and (b) receiver experimental test setup.

At 112 Gbps we measure clean open eyes from the TX PAC, as shown in Fig. 7. We characterize TDECQ out of the transmitter under a variety of scenarios. TDECQ (transmitter and dispersion eye closure quaternary) is a figure of merit for the eye quality of PAM4 optical transmitters [37]. The TX PAC measures an extinction ratio of 3.8 dB and a TDECQ of 2.3 dB with a standard 5-tap feed forward equalizer (FFE) which meets the IEEE 802.3 requirement for a 400GBASE-DR4 transmitter. With the aid of a continuous time linear equalizer (CTLE) analog filter and additional FFE taps, the TX eye opens up further, indicating that an improved |S21| response in a redesigned device would further improve our measured TDECQ. The CTLE filter implemented on the DCA has a 21 GHz zero, 27 GHz first pole, and 32 GHz second pole.
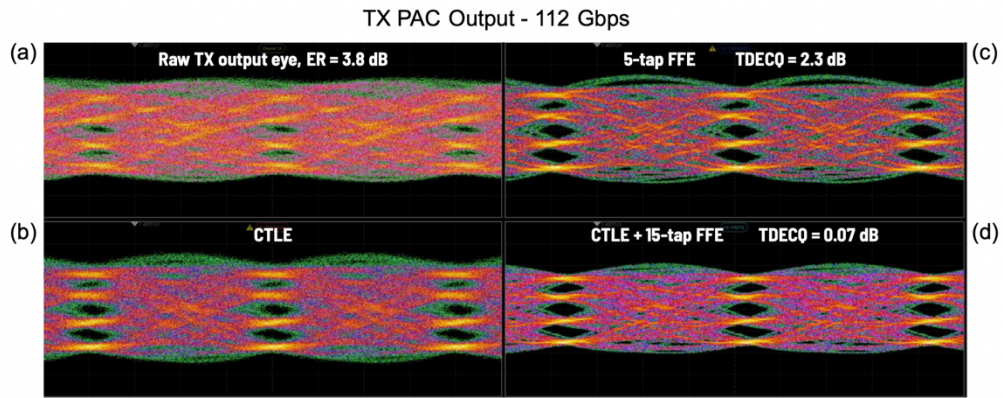

Fig 7. Measured eye diagrams from TX PAC testing at 112 Gbps with various filters implemented on the DCA, sampled with a baud/2 bandwidth receiver: (a) A "raw" TX without further signal processing; (b) processed with an analog CTLE where the CTLE has a 21 GHz zero, 27 GHz first pole, and 32 GHz second pole; (c) with a 5-tap FFE; and (d) with the CTLE and a 15-tap FFE.

Similar to the TX PAC performance, the PAC RX also shows open eyes when tested at 112 Gbps. A modulated signal from the reference modulator with mean power of 1.0 mW is input at the SM fiber. Measured fiber-referred high-speed photodiode responsivity for the assembly under test is 245 mA/W for TE-polarized and 210 mA/W for TM-polarized input light, corresponding to 0.7 dB polarization-dependent loss. Fig. 8 shows the optical input to the PAC RX from the reference modulator in (a), the sampled eye after a baud/2 receiver in (b), and the filtered eye after a feed forward equalizer in (c). At 112 Gbps, only a 5-tap FFE is required to open the eye, well within the capabilities of an LR SERDES. Many long reach SERDES also implement CTLE and/or a decision feedback equalizer, which could further improve performance [38-40].

In operation our modulator driver, TIA, biasing, and active control require 483 mW. At 112 Gbps, this corresponds to 4.3 pJ/bit, not including the laser or SERDES. Future TX PAC devices may incorporate a local undercut, which would reduce the required thermal tuning power. A breakdown of the power consumption is shown in Table 1. All values are measurements except for the heater and associated drive circuitry overhead, which is projected at a required optical phase shift of $\pi/2$ radians.
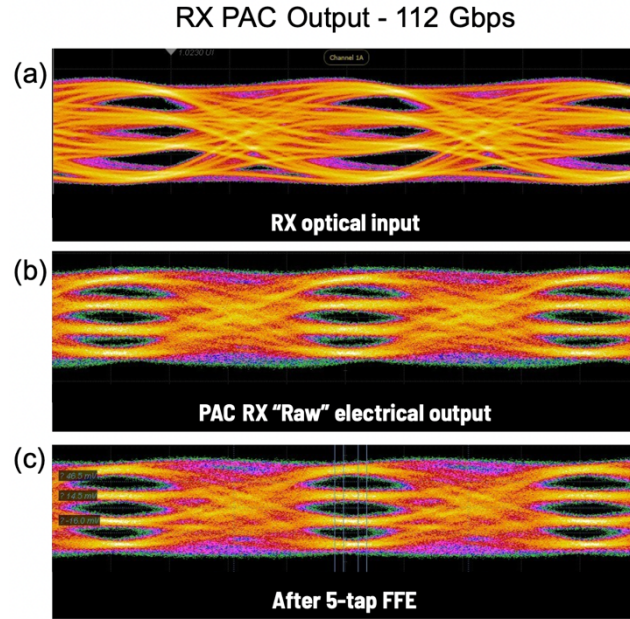

Fig. 8. Measured eye diagrams from RX PAC testing at 112 Gbps. Shown in (a) is the optical input from the reference modulator used as stimulus. (b) Shows the "raw" eye after a baud/2 bandwidth sampler in the DCA and (c) shows the eye after a 5-tap FFE.

Table 1. Breakdown of power consumption for the TX PAC and RX PAC and extrapolation to typical total power consumption for transmitter and receiver

Component	Measured Power Consumption (mW)	Energy Efficiency at 112 Gbps (pJ/bit)
Modulator & driver	312	2.8
TIA	114	1.0
Mixed signal TWMZ control	7.6	0.1
Heater and drive circuitry overhead (Typical)	49[a]	0.4
Total (Typical)	483	4.3

[a] Projected average value for the expected intrinsic phase error to be corrected of $\pi/2$.

4. Conclusion

Monolithic CMOS-silicon photonics processes are attractive platforms for next-generation co-packaged optics applications. A critical unanswered question up to now is whether such platforms are capable of operating at high-speed, particularly in 45 nm CMOS. We demonstrate that such a monolithic platform is suitable for 112 Gbps optical communications. Co-packaging these transmitter and receiver chips with a processor, switch, or other ASIC will ultimately result in improvements in computer system performance per Watt compared to what would be achieved by utilizing conventional pluggable optics.

Disclosures. The authors declare no conflicts of interest.

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